REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 5 to positively recite that each via, including the lower electrode of the capacitor, present in the first dielectric layer has an upper surface that is coplanar to the upper surface of said first dielectric layer. Support for this amendment to Claim 5 is found at Page 9, lines 1-3 as well as in FIG. 12.

Since the above amendment to Claim 5 is fully supported by the originally filed application, entry thereof is respectfully requested.

In the present Office Action, Claim 5 stands rejected under 35 U.S.C. § 102 (e) as allegedly anticipated by U.S. Patent No. 5,563,762 to Leung, et al. ("Leung, et al."). Claim 5 is also rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Leung, et al. and U.S. Patent No. 6,049,103 to Horikawa, et al. ("Horikawa, et al."). Claims 6-8 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Leung, et al., Horikawa, et al. and U.S. Patent No. 5,920,775 to Koh ("Koh").

Concerning the § 102(e) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The

corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the disclosure of Leung, et al. does not anticipate the claimed structure recited in amended Claim 5. Specifically, Leung, et al. do not disclose an interconnection wiring system containing at least one capacitor comprising: a substrate having a planar upper surface of insulating and conductive regions therein, a first level of interconnection wiring interconnecting said conductive regions, a first dielectric layer formed over said first level of interconnection wiring, said first dielectric layer having an upper surface and having vias therein filled with conductive material to said upper surface and in contact with regions of said first level of interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer*, a second dielectric layer formed over said lower electrode and extending beyond the perimeter of said lower electrode, and a second level of interconnection wiring interconnecting the vias filled with conductive material and formed over the second dielectric layer to form said top electrode of said capacitor.

Leung, et al. provide a capacitor structure including a bottom electrode, a capacitor dielectric and a top electrode that are formed on a passivation layer overlying interconnect metallization. Specifically, FIGS. 3 and 4 illustrate capacitor structures disclosed in Leung, et al. In FIG. 3, the capacitor 100 comprises bottom electrode 128, capacitor dielectric 130 and top electrode 134, which is situated on a passivation layer

116 that is present atop a first dielectric 114 that has open vias 118 and conductively filled vias 124 located therein. In FIG. 4, the capacitor 200 includes a bottom electrode 228, a capacitor dielectric 230 and a top electrode 34 that is situated atop a passivation layer 216. The passivation layer 216 is located atop a dielectric 214 that has open vias 218 and vias that include the capacitor 200.

The capacitor structures disclosed in Leung, et al. do not include a first dielectric layer formed over said first level of interconnection wiring, where the first dielectric layer having an upper surface and having vias therein filled with conductive material to said upper surface and in contact with regions of said first level of interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer*, as presently claimed. The dielectric layer 114 or 214 in Leung, et al. does not include the features mentioned above.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Leung, et al. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the obviousness rejection to Claim 5 citing Leung, et al. and Horikawa, et al., applicants respectfully submit that these combined prior art references do not render the claimed structure obvious. Specifically, the combined disclosures of Leung, et al. and Horikawa, et al. do not teach or suggest an interconnect structure

including applicants' claimed first dielectric layer formed over said first level of interconnection wiring, said first dielectric layer having an upper surface and having vias therein filled with conductive material to said upper surface and in contact with regions of said first level of interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer.*

Leung, et al. are defective for the same reason mentioned above in connection with the anticipation rejection. Applicants thus incorporate thus remarks herein by reference. To reiterate: Leung, et al. do not teach or suggest an interconnect structure including, among other components, a first dielectric layer formed over said first level of interconnection wiring, said first dielectric layer having an upper surface and having vias therein filled with conductive material to said upper surface and in contact with regions of said first level of interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer.* As stated above, the dielectric layer 144 or 214 of Leung, et al. does not include the claimed features recited in amended Claim 5.

The above defects in Leung, et al. are not alleviated by Horikawa, et al. since the applied secondary reference also does not teach or suggest a structure including applicants' claimed first dielectric layer formed over said first level of interconnection wiring, where said first dielectric layer has an upper surface and vias therein filled with conductive material to said upper surface and in contact with regions of said first level of

interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer*. Applicants observe in the first instance that the Examiner has referred to FIGS. 34-42 of Horikawa, et al. in forming the rejection. Thus, applicants' comments are made to those figures since they appear to be the closest to the claimed invention. In accordance with Horikawa, et al., dielectric 110 includes a conductively filled via 110a that has a lower electrode 114 including layers 134 and 135 on the conductively filled via within the first dielectric layer 110. This structure does not, however, include applicants' claimed dielectric layer *wherein each via, including the lower electrode of the capacitor, has an upper surface that is coplanar to the upper surface of the dielectric layer*. In the prior art, the lower electrode is atop the via thus the two components do not have upper surfaces that are both coplanar to the upper surface of the dielectric, as presently claimed.

Based on the above remarks, the rejection to Claim 5 citing the combined disclosures of Leung, et al. and Horikawa, et al. under § 103 has been obviated. Reconsideration and withdrawal of the instant obviousness rejection are thus respectfully requested.

Insofar as the obviousness rejection to Claims 6-8 citing the combined disclosures of Leung, et al., Horikawa, et al. and Koh is concerned, applicants respectfully submit that these applied references do not render the claimed structure recited in amended Claim 5 obvious. Specifically, the combination of Leung, et al., Horikawa, et al. and Koh does not teach or suggest a structure including, among other components, a first dielectric layer formed over said first level of interconnection wiring, said first dielectric layer

having an upper surface and having vias therein filled with conductive material to said upper surface and in contact with regions of said first level of interconnection wiring, *wherein at least one of said vias having dimensions to form said lower electrode of a capacitor and each via, including said lower electrode of said capacitor, has an upper surface that is coplanar to said upper surface of said first dielectric layer.*

The deficiencies in regard to the combined disclosures of Leung, et al. and Horikawa, et al. discussed above are applicable here for this rejection. Thus, the above remarks regarding Leung, et al. and Horikawa, et al. are incorporated herein by reference.

Koh does not alleviate the above defects in Leung, et al. and Horikawa, et al. since it also does not teach or suggest a structure including the claimed first dielectric layer. In Koh, the capacitor including lower electrode 26c, capacitor dielectric 32 and upper electrode 44d is located atop a first dielectric 20e. Conductively filled vias are present in the first dielectric. The prior art structure does not include the planarity between the vias, lower electrode and the first dielectric that is recited in the claims of the present application.

Based on the above remarks, the rejection to Claims 4-6 citing the combined disclosures of Leung, et al., Horikawa, et al. and Koh under § 103 has been obviated. Reconsideration and withdrawal of the instant obviousness rejection are thus respectfully requested.

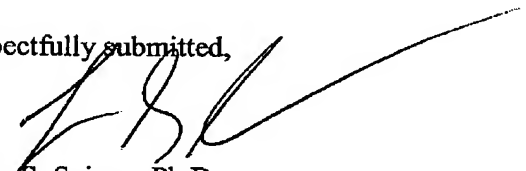
The § 103 rejections also fails because there is no motivation in the applied references which suggest modifying the disclosed structure to include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification

mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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